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Damage-free finishing of CVD-SiC by a combination of dry plasma etching and plasma-assisted polishing

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ABSTRACT

To realize the damage-free finishing of CVD-SiC substrates, which are used as materials for space telescope mirrors and glass lens molds, plasma chemical vaporization machining (PCVM) and plasma-assisted polishing (PAP) were combined. In this study, the properties of such CVD-SiC substrates, including their surface morphology, composition and crystalline orientation, were investigated. Lapping using diamond abrasives and conventional chemical mechanical polishing (CMP) using CeO_2 slurry were conducted for comparison with the proposed atmospheric-pressure-plasma-based finishing process. Many scratches and a subsurface damage (SSD) layer were formed by the diamond lapping of CVD-SiC. Conventional CMP using CeO_2 slurry was conducted for the damage-free finishing of CVD-SiC. However, the polishing efficiency was very low. In the proposed process, PCVM, which is a noncontact dry etching process, was performed to remove the SSD layer while PAP, which combines plasma modification and soft abrasive polishing, was performed for damage-free surface finishing. PCVM was conducted on a diamond-lapped CVD-SiC surface. After PCVM for a short duration of 5 min, the scratches and SSD layer formed by lapping were completely removed, although the surface roughness was slightly increased. PAP using a resin-bonded CeO_2 grindstone was conducted to decrease the surface roughness of CVD-SiC processed by diamond lapping and PCVM for 5 min, for which a loose-held-type grindstone was demonstrated to be very useful. A flat and scratch-free surface with an rms roughness of 0.6 nm was obtained after PAP finishing.

1. Background

Materials with a high hardness, light weight and high thermal conductivity are very suitable for space telescope mirrors and glass lens molds, making chemical vapor deposition silicon carbide (CVD-SiC) one of the most promising materials for such applications [1–3]. Compared with tungsten carbide and reaction sintered SiC, CVD-SiC has a higher hardness, meaning that CVD-SiC has strong resistance to wear due to abrasion and making it difficult to form scratches and subsurface damage (SSD) in the abrasive polishing of CVD-SiC. Also, CVD-SiC has high durability against high-temperature oxidation, thus long-life mold applications can be expected. Moreover, it has high thermal conductivity and a low thermal expansion coefficient, making the likelihood of shape failures caused by nonuniformity of the temperature distribution in the molding process very small.

Although CVD-SiC is very suitable for use in space telescope mirrors and glass lens molds, its poor machinability due to its high hardness and chemical inertness greatly limits its practical applications. To use CVD-SiC as a substrate for telescope mirrors and glass lens molds, high-quality surfaces with no SSD layers, scratches or cracks are indispensable as well as nanometer-level surface shape accuracy and subnanometer-level surface roughness. Currently, conventional machining processes such as grinding, lapping and chemical mechanical polishing (CMP) are widely used for the figuring and finishing of CVD-SiC [4–7]. However, in the grinding and lapping processes, diamond abrasives are used. Thus, scratches, SSD and micro pits, which deteriorate the properties of the substrate, are inevitably introduced. On the other hand, when CMP is used for the damage-free finishing of CVD-SiC, the material removal rate (MRR) is extremely low. Moreover, the use of slurry is not environmentally friendly and increases the cost of finishing owing to the management and post-treatment of slurry. For the practical application of CVD-SiC, low cost, damage-free and highly efficient figuring and finishing techniques for CVD-SiC are essential.

To overcome the problem of the poor machinability of CVD-SiC, an atmospheric-pressure (AP)-plasma-based figuring and finishing process based on the combination of PCVM and PAP is proposed for the damage-free finishing of CVD-SiC. As a highly efficient and damage-

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free figuring technique, PCVM was proposed for the figuring of Si-based substrates [8,9]. PCVM is a noncontact etching process, thus SSD is not introduced during figuring. In our previous research, PCVM was widely applied for the figuring of X-ray mirrors made of Si and for the thickness correction of quartz crystal wafers and nanometer-level shape accuracy and thickness uniformity have been achieved [8,9]. On the other hand, PAP, in which surface modification by plasma irradiation and the removal of the modified layer by soft abrasives are combined, has been proposed for the finishing of some difficult-to-machine materials [10–13]. In our previous research, PAP using CeO_2 as an abrasive was successfully used to finish the surface of single-crystal SiC (0001) and a reaction-sintered SiC ceramic [10,14], and scratch-free and damage-free surfaces were obtained. In particular, in the case of single-crystal SiC, an atomically flat surface with a well-ordered step-terrace structure was generated [10]. In this study, PCVM, which is a noncontact dry etching process, will be used to efficiently remove the SSD layer, and PAP, which has a good finishing ability for hard materials, will be used to decrease the surface roughness. It is expected that a damage-free and smooth CVD-SiC surface can be obtained using this combined finishing process.

2. CVD-SiC used in this study

CVD-SiC is usually grown on other substrates such as RS-SiC, graphite and so forth. Among different CVD-SiC manufacturers, even though their growth processes have the same mechanism, the growth parameters, such as the temperature, pressure, and gas flow rates, are considerably different. Therefore, CVD-SiC substrates from different manufacturers may have different properties such as purity, crystallinity, surface morphology and so forth. The CVD-SiC substrates used in this study were supplied by Tokai Fine Carbon Co. Limited.

Fig. 1(a) shows a photograph of a CVD-SiC substrates used in this study. SiC was grown on both sides of a graphite substrate and the thickness of the CVD-SiC layer was about 100 μm. Fig. 1(b) shows a scanning white light interferometer (SWLI) image of the substrate. No flattening process was conducted after CVD growth. Therefore, the surface is very rough. As shown in the scanning electron microscope (SEM) image of Fig. 1(c), the SiC grains in the substrate are very small (less than 1 μm in diameter). It is considered that the smaller the SiC grains, the better the properties obtained, such as low surface roughness after polishing, high hardness and high strength. Therefore, it was assumed that excellent properties can be obtained using this substrate.

In PCVM and PAP, material removal is based on chemical reactions between radicals in the plasma and the substrate [8,10]. Thus, it is necessary to investigate the composition and crystalline orientation of the CVD-SiC substrates used in this study. X-ray photoelectron spectroscopy (XPS) measurements were conducted to investigate the surface composition. Wide-scan XPS spectra revealed that only Si, C and O exist in the CVD-SiC layer. Fig. 2 shows the peak separation results of narrow-scan spectra of C1s, O1s and Si2p. As indicated by the O1s and Si2p spectra, a thin oxide layer was observed, which is considered to be due to the native oxide. Also, as shown in the C1s spectrum, a small amount of organic contamination (C-C/C-H) exists on the substrate surface.

The crystalline orientation of the SiC layer was investigated by X-ray diffraction (XRD). The XRD pattern is shown in Fig. 3, which indicates very high crystallinity of the substrate. Two obvious char-

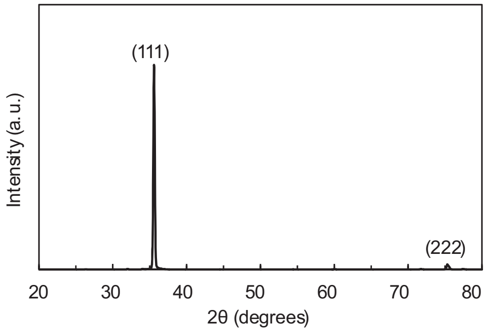
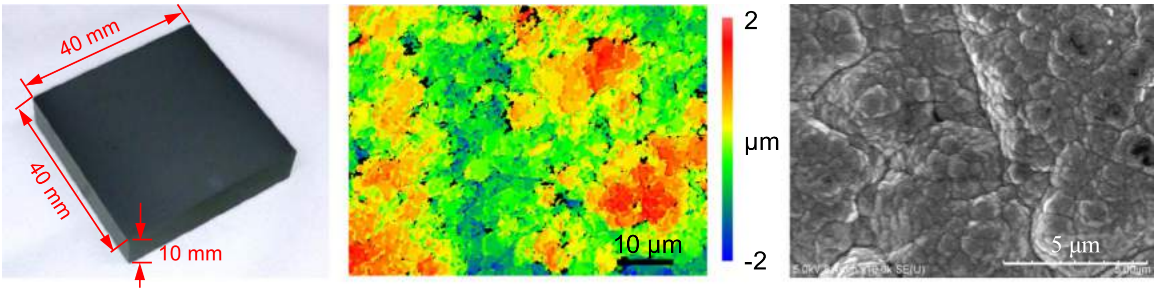


Fig. 3. XRD pattern of the CVD-SiC substrate.



(a) (b) (c)

Fig. 1. CVD-SiC substrate used in this study. (a) Photograph. (b) SWLI image (p-v: 4643.5 nm, rms: 621.0 nm). (c) SEM image.

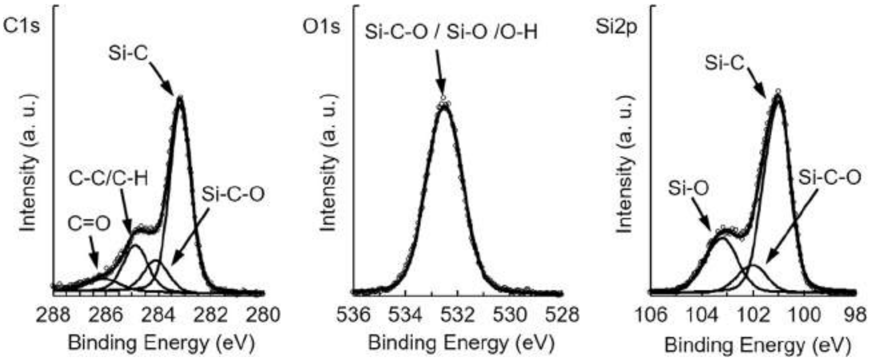


Fig. 2. XPS spectra of the CVD-SiC substrate.

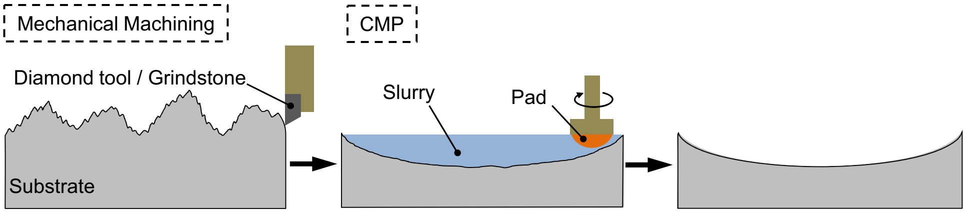


Fig. 4. Schematic view of conventional figuring and finishing processes of CVD-SiC.

acteristic peaks at 35.7° and 73.8°, corresponding to the diffraction from the (111) and (222) crystal planes of β-SiC [15], respectively were observed. This means that the SiC grains in the CVD-SiC substrate have a phase structure of β-SiC and that almost all the grains are highly oriented.

3. Conventional lapping and CMP of CVD-SiC

CVD-SiC has a very high hardness, which makes it difficult to mechanically process. Therefore, for the figuring of CVD-SiC, diamond tools are used for turning and diamond grinding stones are used for grinding [4–7]. Fig. 4 shows a schematic view of the conventional figuring and finishing processes of CVD-SiC. After figuring using mechanical methods, finishing using CMP is usually conducted to remove the SSD formed by the previous mechanical processes and decrease the surface roughness.

Diamond lapping was conducted on a CVD-SiC substrate under the conditions shown in Table 1. Since there were components with a large spatial wavelength on the as-grown surface, the polishing time was set to a quite long duration to smooth the whole substrate surface. Fig. 5 shows SWLI and SEM images of the lapped surface. Even though the surface roughness was greatly decreased to a mirror level, deep scratches can be observed in the SWLI image and a large number of shallow scratches were formed as shown in the SEM image. In our previous study on the finishing of single-crystal SiC, the diamond lapping of 4H-SiC (0001) was also conducted under the same conditions, and an SSD layer with a thickness of about 100 nm was formed [16]. Therefore, it is considered that there was also a thick SSD layer on the CVD-SiC surface after lapping.

Table 1
Conditions of conventional diamond lapping and CMP of CVD-SiC.

	Diamond lapping	CMP
Load	4000g	200g
Polishing media	Diamond platen	CeO_2 slurry
	Grain size: 5–15 µm	Concentration: 40 wt% Abrasive size: 190 nm Pad: Swede type (ϕ =10 mm)
Rotation speed	Platen: 150 rpm Substrate: 350 rpm	Pad: 2000 rpm
Time	48 h	2+5 h

The formed scratches deteriorate the surface roughness and figure accuracy of the substrate surface, which will affect the performance of mirrors and molds. Also, the SSD layer will affect the durability of these components. Therefore, it was concluded that diamond lapping is not a suitable finishing method for CVD-SiC and that a damage-free finishing technique with a high efficiency and low cost is required.

CMP is widely used as a damage-free finishing technique for semiconductor and optical components [17,18]. CMP using CeO_2 slurry was conducted on an as-grown CVD-SiC substrate under the conditions shown in Table 1. A high slurry concentration, a high polishing pressure and a high pad rotation speed were applied to realize a high polishing efficiency in accordance with Preston's law [19]. Fig. 6 shows the CMP-processed surfaces after different durations of CMP. After CMP for 2 h, the surface roughness was decreased but the surface was still very rough as shown in Fig. 6(a). After CMP for an additional 5 h, a flatter surface was obtained but the surface roughness was still unsatisfactory for applications such as mirrors and mold components. As shown in Fig. 6(c), even after CMP for 7 h, there were still many unpolished areas on the surface. The CMP of CVD-SiC using commercially available SiO_2 slurry was also conducted and very similar results were obtained. This means that the efficiency of CMP for CVD-SiC is very low, making CMP a time-consuming and high-cost finishing process.

4. AP-plasma-based finishing of CVD-SiC

4.1. Concepts of PCVM and PAP

An AP-plasma-based process is proposed to realize the highly efficient, low-cost and damage-free finishing of CVD-SiC. Fig. 7 shows a schematic view of the proposed concept. Regarding the figuring stage, conventional mechanical methods such as turning and grinding using diamond are used to realize figuring with a low cost and high efficiency. However, scratches and SSD are inevitably formed since diamond tools or grinding wheels are used in the figuring stage. Thus, PCVM, which is a chemical dry etching process, is used for the removal of the scratches

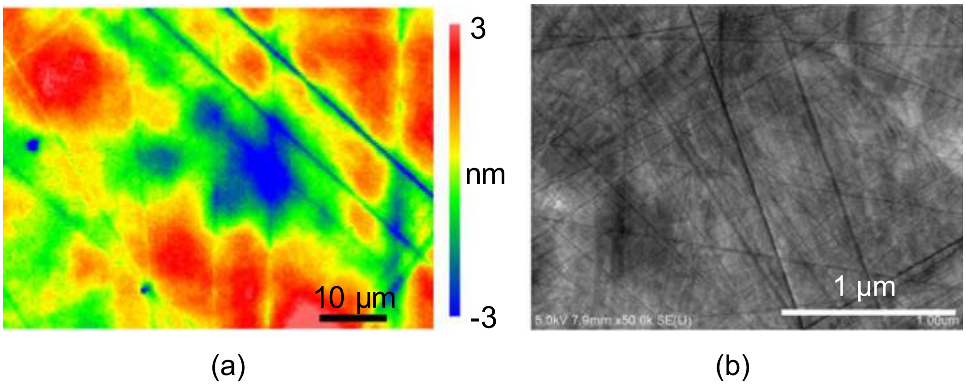


Fig. 5. CVD-SiC surfaces after diamond lapping. (a) SWLI image (p-v: 24.86 nm, rms: 1.16 nm). (b) SEM image.

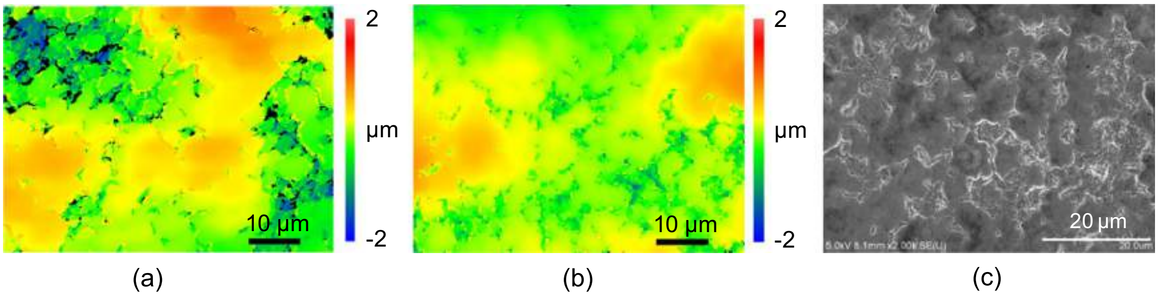


Fig. 6. CMP-processed CVD-SiC surfaces. (a) SWLI image after CMP for 2 h (p-v: 3517.0 nm, rms: 457.1 nm). (b) SWLI image after CMP for 7 h (p-v: 2571.1 nm, rms: 312.8 nm). (c) SEM image after CMP for 7 h.

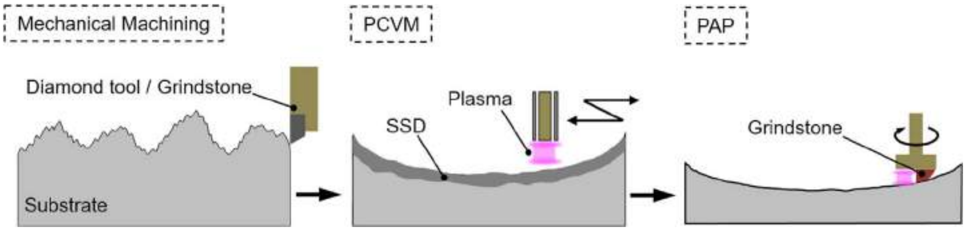


Fig. 7. Schematic view of the plasma-based damage-free finishing process of CVD-SiC.

and the SSD layer. Etching in PCVM is isotropically performed and an ultrasmooth surface with subnanometer surface roughness cannot be obtained using PCVM only. Thus, PAP is conducted for damage-free final finishing to decrease the surface roughness.

The experimental setup of PCVM is shown in [20]. To realize the etching of SiC, He-based CF4 was used as the plasma gas. The diameter of the powered electrode, which was made of aluminum alloy, was 3 mm. Atmospheric-pressure He-based CF4 plasma was generated by applying a 13.56 MHz radio frequency (RF) power between the electrode and the stage. In CF_4 plasma, the CF4 molecules dissociated as a result of electron impact. Thus, a large number of F radicals were generated in plasma and they reacted with the SiC and etched the surface.

PCVM is a non-contact figuring process with a very high efficiency [8,9]. Therefore, it is considered that the SSD and scratches formed by previous mechanical processes can be completely removed by PCVM in a very short time without the formation of further damage.

For final finishing after PCVM, PAP, which is a dry polishing technique without the use of slurry, was conducted. Water vapor plasma was used in the PAP of CVD-SiC. Hydroxyl radicals with a high oxidation potential were generated by the dissociation of water molecules. SiC grains in CVD-SiC were oxidized by the irradiation of water vapor plasma, and the oxide layer, which was much softer than the SiC, could be removed by polishing using a soft grinding stone [10,11]. Thus, damage-free surface finishing could be realized.

Fig. 8 shows schematic views of the PAP setup and an enlarged image of the polishing tool. A resin-bonded grinding stone (ϕ 8 mm) was fixed on the bottom of an electrode (ϕ 20 mm), which was made of Al alloy with an offset of 4 mm from the rotation center. A mixture of He and water vapor, which was used as the process gas for plasma generation, was supplied into the glass cover and flowed through the space between the electrode and the substrate. The gap between the electrode and the substrate was 1 mm. Water-vapor-containing plasma was generated around the grinding stone by applying an RF power between the electrode and the stage. With the rotation of the electrode under a constant load, which could be adjusted via the weight, plasma modification and abrasive dry polishing were simultaneously conducted.

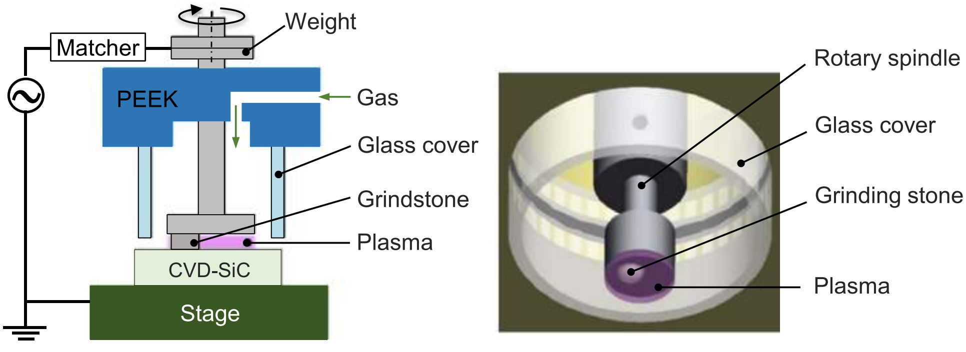
4.2. PCVM of CVD-SiC

As shown in Fig. 1, the CVD-SiC layer consists of SiC, SiO_2 (native oxide) and contamination (C-C/C-H). In PCVM, CF_4 plasma was used to etch the substrate surface on the basis of the following reactions.

$$SiC + CF_4 + O_2 \rightarrow 2CO\uparrow + SiF_4\uparrow \quad (1)$$

$$SiO_2 + CF_4 \rightarrow CO_2\uparrow + SiF_4\uparrow \quad (2)$$

$$C_xH_y + O/OH/F \rightarrow CO/CO_2/H_2O/CF_4\uparrow \quad (3)$$



(a)

(b)

Fig. 8. (a) Schematic view of the PAP setup. (b) CAD image of the polishing tool.

It is found that when CVD-SiC is irradiated by CF_4 plasma, chemical reactions occur and all the reaction products are volatile. Therefore, the etching of CVD-SiC using CF_4 plasma is possible.

Table 2 shows the experimental parameters used in PCVM. The raster scanning of localized plasma was conducted on the substrate. The surface after PCVM was observed by SEM. Fig. 9 shows the observation results. Compared with the as-received surface shown in Fig. 1(c), the surface became smoother with the increase in the removal depth. However, many small particles with a size of 10 nm order were observed as shown in Fig. 9(c).

It is considered that these small particles originated from the nonvolatile reaction products generated in the PCVM process. To clarify the composition of these small particles, XPS measurements of PCVM-processed surfaces were conducted. Fig. 10 shows the peak separation of the F1s spectrum measured on the PCVM-processed surface. It was confirmed that these particles are carbon fluorides (C_xF_y), which were generated in the PCVM process [21]. These residual particles increased the surface roughness. Therefore, the conditions of PCVM needed to be optimized to suppress the generation of such residual particles.

Taking the composition of these particles into consideration, it is assumed that the addition of O_2 to the reactive gas will be effective for removing these particles. This is because O_2 will be dissociated in the plasma area to generate O radicals, which will react with the carbon fluorides and remove them by the reaction:

$$C_xF_y + O \rightarrow CO/CO_2/F\uparrow \cdot \quad (4)$$

The above assumption was experimentally confirmed. PCVM with 2 sccm O_2 as an additive was conducted with the other parameters given in Table 2. Fig. 11 shows a SEM image of the processed surface. The surface is very smooth and no C_xF_y residual particles can be observed. This means that O_2 is a very useful additive for preventing the

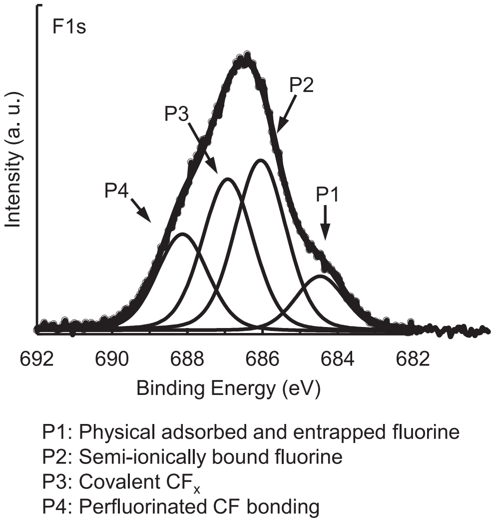


Fig. 10. XPS measurements of PCVM-processed CVD-SiC surface (F1s spectrum).

Table 2
Conditions of PCVM without addition of O_2.

RF power	20, 30 W
Gas flow rate	He: 1.0 slm, CF_4: 20 sccm
Scanning speed	5 mm/s
Feed pitch	0.5 mm
Processing time	30 min

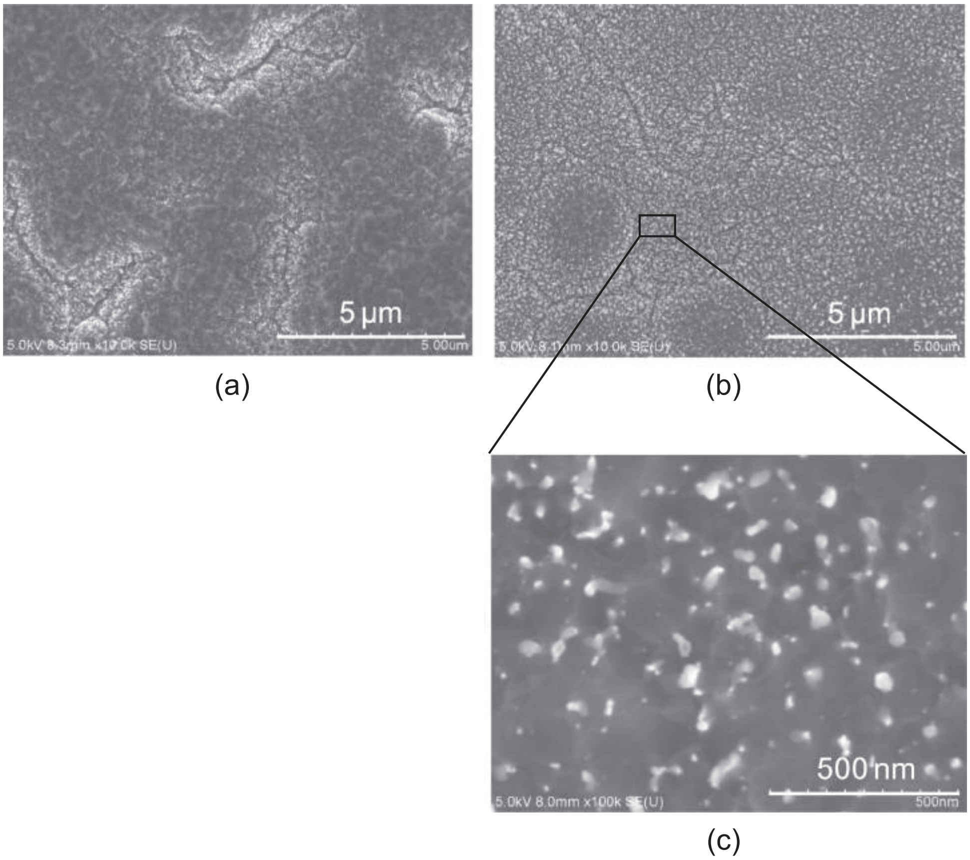


Fig. 9. SEM images of PCVM-processed CVD-SiC surface. (a) Applied power: 20 W. (b) Applied power: 30 W. (c) An enlarged image.

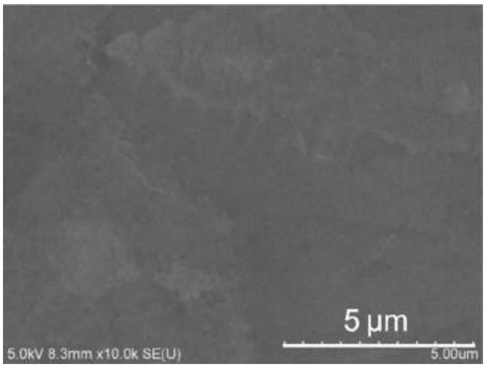


Fig. 11. SEM image of PCVM-processed CVD-SiC surface with the addition of O_2.

generation of C_xF_y particles as assumed. On the basis of the above results, He-based CF_4 and O_2 were used as the plasma gas for the PCVM of CVD-SiC in the following PCVM experiments.

PCVM is mainly conducted to remove the SSD formed by previous mechanical processes. The thickness of the SSD varies with the machining conditions. In a typical figuring process using turning or grinding, SSD with micrometer thickness is formed [22,23]. Therefore, a high MRR is required for PCVM to remove the SSD with high efficiency. The static etching of CVD-SiC for 30 min was conducted with an RF power of 20 W and the addition of 2 sccm O_2 to the plasma gas to evaluate the MRR of PCVM. Fig. 12 shows an SWLI image of the removal spot as well as its cross section, which can be considered as the removal footprint of PCVM. It was confirmed that PCVM has a very high MRR of about 14 μm/h, which is much higher than that of the conventional CMP process for SiC.

Even though PCVM has a very high MRR, it is considered that the surface of a CVD-SiC substrate subjected to PCVM will become rough since PCVM is an isotropic etching process. The PCVM of a diamond-lapped CVD-SiC substrate was conducted for different durations with the experimental parameters shown in Table 2, an RF power of 20 W and the addition of 2 sccm O_2 to the plasma gas. Fig. 13 shows SWLI images of PCVM-processed CVD-SiC surfaces and a graph indicating the change in the rms roughness with the duration of PCVM. After PCVM for a short time (5 min), the scratches formed by diamond lapping completely disappeared even though the surface roughness also increased as assumed. It is clear that the surface roughness increased with the duration of PCVM. In this study, the thickness of the SSD layer introduced by diamond lapping was confirmed by cross sectional transmission electron microscopy. However, due to the polycrystalline structure of CVD-SiC, the SSD layer couldn't be clearly observed. In previous research, a similar lapping process was conducted on a single crystal SiC (0001) substrate after which a SSD layer with a thickness of about 100 nm was introduced [16]. It was assumed that a SSD layer with similar thickness was introduced after diamond lapping of CVD-SiC. Taking the MRR of PCVM and the probable thickness of the SSD layer into consideration, PCVM for 5 min was sufficient to completely remove the SSD formed by diamond lapping. Therefore, the surface shown in Fig. 13(a) is considered to be damage-free. To decrease the roughness of this damage-free surface, additional finishing is required.

4.3. PAP of CVD-SiC

The surface processed by PCVM for 5 min shown in Fig. 13(a) was finished by PAP, in which plasma modification and abrasive dry polishing were combined. Water vapor plasma was used in this work. A large amount of hydroxyl radicals with a high oxidation potential were generated in water vapor plasma and CVD-SiC could be oxidized just as what occurred with 4H-SiC after water vapor plasma irradiation [10]. SiC was oxidized to silicon dioxide which was much softer than SiC, making it possible to polish the plasma-irradiated surface using soft abrasives.

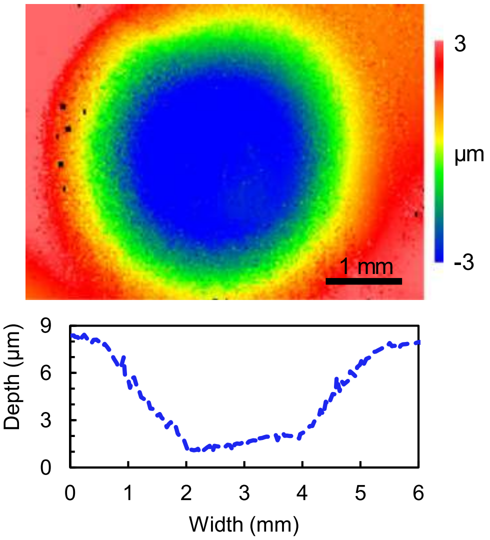


Fig. 12. SWLI image and cross-sectional of the removal footprint in PCVM.

To realize damage-free finishing, resin-bonded CeO_2 grinding stones were used. Both of the abrasive material (CeO_2) and the bonding material (resin) are much softer than SiC, thus, it was considered that only the oxide layer could be removed while SSD layer could not be formed in PAP. Two types of grinding stone, a regular fixed-type and a loose-held-type, were investigated. Fig. 14 shows SEM images of these two types of grindstone. The average diameter of the CeO_2 grains was 0.7 μm.

Table 3 shows the conditions of PAP. When the regular fixed-type grindstone was used in PAP, hardly any polishing occurred owing to its very rapid abrasion in PAP. It was considered that the parameters of the fixed-type grinding stones needed to be optimized, such as the concentration of CeO_2 grains, the grain size, the structure of the resin and so forth. In the case of the loose-held-type grindstone, PAP was effectively conducted. Fig. 15 shows an SWLI image of the polished CVD-SiC surface after PAP for 3 h using the loose-held-type grinding stone. The protrusions existing on the PCVM-processed surface shown in Fig. 13**(a)** were completely removed and a smooth surface was obtained. The surface rms roughness over a 64 μm×48 μm area was also improved from 2.93 to 0.69 nm.

4.4. Discussions

As shown in Fig. 11, a smooth surface with no C_xF_y residual particles was obtained after adding O_2 into the plasma gas. However, as an electron-negative gas, addition of O_2 may probably decrease the radical density of plasma and further decrease the plasma etching efficiency. Thus, the amount of additive O_2 should be optimized in the future research. Meanwhile, other conditions including the electrode gap, applied RF power, CF_4 concentration and so forth also need to be optimized in order to obtain a high plasma etching rate so that the required time of PCVM to remove the SSD layer can be decreased. As shown in Fig. 13, with the increase of the duration of PCVM, the surface roughness also increased which means longer finishing time is

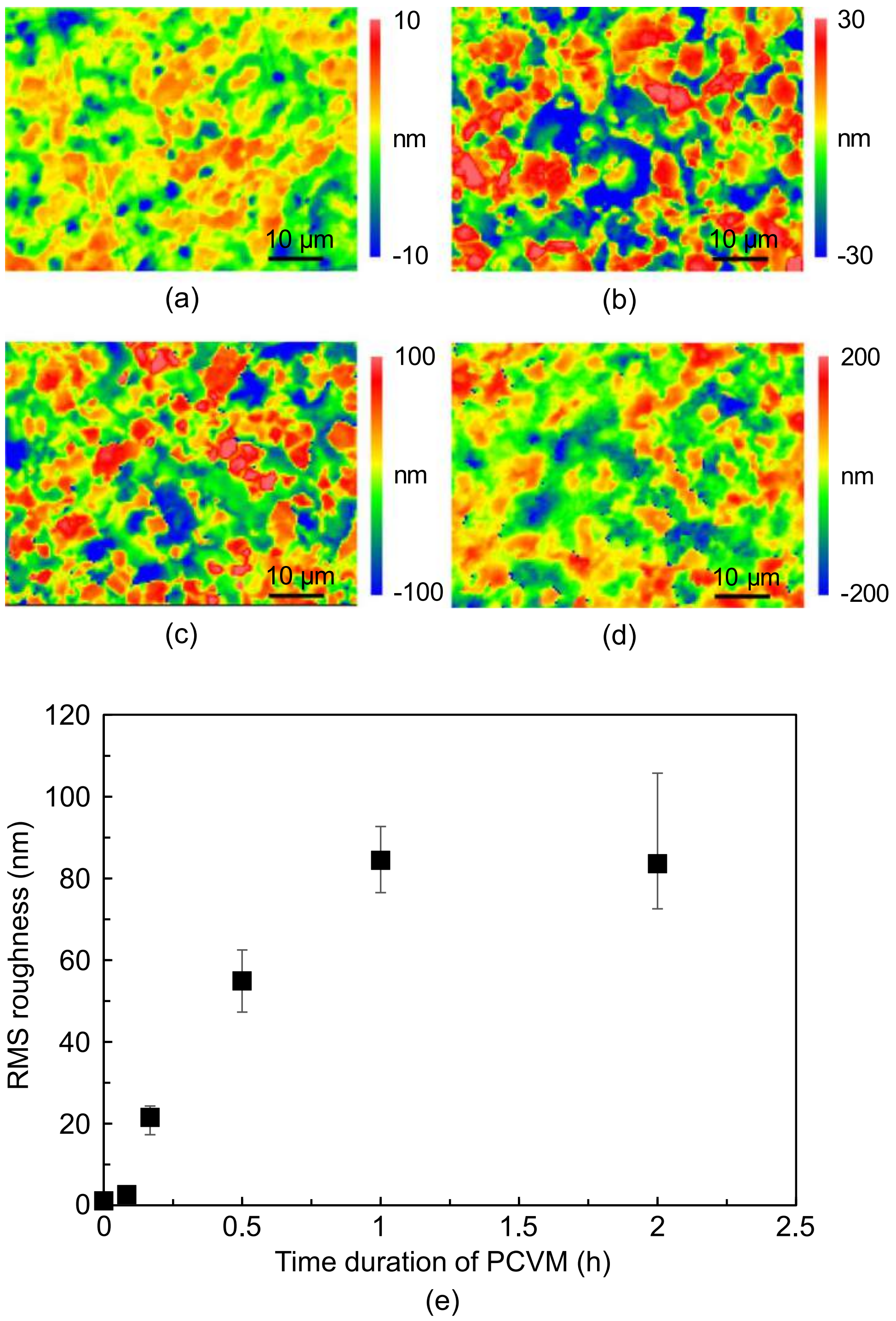


Fig. 13. (a-d) SWLI images of PCVM-processed surfaces with different processing time. (a) 5 min (b) 10 min (c) 30 min (d) 1 h. (e) Change of rms roughness with the increase of duration of PCVM.

required for the following PAP process. Thus, improvement of the removal efficiency of PCVM can help to decrease the duration of the whole finishing process.

After PAP using the loose-held-type grindstone, it was found that the resin in the grindstone was oxidized owing to the high friction heat in the area of contact between the grindstone and the substrate during abrasion. That is to say, resin with stronger heat resistance should be used in PAP. Also, the deterioration of the grindstone surface was confirmed after polishing. Therefore, a dresser that can be applied in the PAP of CVD-SiC substrates should be developed in the future research. Meanwhile, the relationship between the grain size of CeO_2 and the surface roughness will also be investigated.

In this feasibility study, the combination of PCVM and PAP has been proved to be very useful for the damage-free finishing of CVD-SiC. However, for the application as the substrate material for space telescope mirrors and glass lens molds, aspheric surfaces should be finished. The experimental setup shown in Fig. 8 was used for a fundamental study of PAP, for which only a localized plane area can be polished. Therefore, a PAP machine that can be practically used for finishing the curved surfaces of substrates with different sizes will be

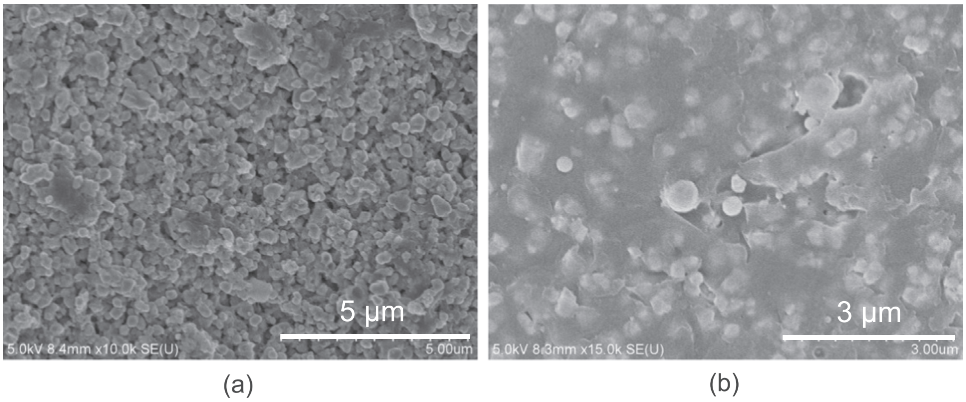


Fig. 14. SEM images of the grindstones. (a) Regular fixed-type. (b) Loose-held-type.

Table 3
Conditions of PAP of CVD-SiC.

RF power	15 W
Gas flow rate	He of the main path: 1.5 slm He of the sub-path bubbled through a water contained bottle: 20 sccm
Grindstone	CeO_2 (fixed-type, loose-hold-type)
Abrasive size	0.7 µm
Load	180g
Rotation speed	500 rpm
Processing time	3 h

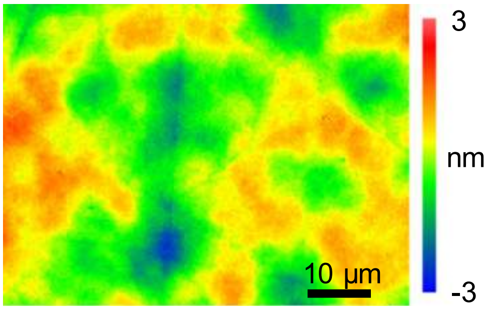


Fig. 15. SWLI image of the PAP-processed surface using a loose-hold-type grinding stone (p-v: 4.41 nm, rms: 0.69 nm).

developed in our future study.

5. Conclusions

To realize the damage-free finishing of CVD-SiC substrates, which are used as materials for space telescope mirrors and glass lens molds, PCVM and PAP were combined. The properties of the CVD-SiC substrates used in this study were investigated. The as-grown surface of the CVD-SiC substrate was very rough and its surface composition was determined by XPS, which indicated that a thin oxide layer and a contamination layer existed. The high crystallinity of the substrate was proved by XRD measurements and all the SiC grains had the same (111) surface orientation.

(1) PCVM was conducted on a diamond-lapped CVD-SiC surface. It was found that the addition of O2 into the plasma gas could effectively preventing the generation of carbon fluoride particles. Meanwhile, the etching rate of PCVM was measured to be 14 µm/h, which was much higher than other conventional finishing methods. After PCVM for a short duration of 5 min, the scratches and SSD layer formed by lapping were completely removed, although the surface roughness was slightly increased.

(2) PAP using a resin-bonded CeO_2 grinding stone was conducted to decrease the surface roughness of CVD-SiC processed by diamond lapping and PCVM for 5 min, for which a loose-held-type grinding stone was demonstrated to be very useful. A flat and scratch-free surface with an rms roughness of 0.69 nm was obtained.

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